Luyi Li

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OVERVIEW

I am a senior student majoring in VLSI Design and System Integration at Nanjing University. My research interests primarily lie in the field of computer architecture. I have worked on research topics in **secure computer architecture** and **domain-specific acceleration**. In addition, I am interested in heterogeneous computing, in-memory computing, hardware/software co-design and multi-core processors.

EDUCATION

Nanjing University, Nanjing, Jiangsu, China — Sep 2018 – Jul 2022 (Expected)

School of Electronic Science and Engineering

- B.E. in VLSI Design and System Integration
- **Cumulative GPA:** 4.47 / 5.00 (89.4 / 100) (Top 10% in the school)
- **Relevant Courses:** Analog IC Design (95.5), Digital IC Design (94), Embedded Development (92), Digital Signal Processing (92), Digital Image and Computer Vision (92), Introduction to Computer System (90), Principles and Techniques of Compilers (in progress), Computer Organization and Design (in progress), Computer Architecture (Prof. Onur Mutlu's open course)
- **Honors & Prizes:** People Scholarship (2019 & 2020), Jinxiao Scholarship (2021), Outstanding Member of ESE Student Union (2019)

RESEARCH EXPERIENCE

PREFENDER: A Prefetching Defender against Cache Side Channel Attacks (DATE'22)

1st author, Accepted — Mar 2021 – Sep 2021

Advisors: Prof. Zhongfeng Wang and Dr. Lang Feng

- **Motivation:** Cache side channel attacks steal secret information by exploiting hardware vulnerabilities in modern architectures. Existing countermeasures suffer from performance reduction.
- **Overview:** Designed PREFENDER, a secure prefetcher that is able to defeat cache side channel attacks while maintaining or even improving performance.
- **Contribution:** Designed a run-time analytical tracker to learn from past memory access patterns and predict vulnerable addresses subject to attack; Utilized the hardware prefetcher to bring these addresses into cache in advance to obfuscate attackers.
- **Results:** Achieved high security effectiveness under Flush+Reload, Evict+Reload and Prime+Probe attacks, and a performance speedup for the SPEC CPU 2006 benchmark.

PipeBSW: A Two-Stage Pipeline Structure for Banded Smith-Waterman Algorithm on FPGA (ISVLSI'21)

1st author, Best paper nominee — Jul 2020 – Mar 2021

Advisors: Prof. Zhongfeng Wang and Prof. Jun Lin

- **Motivation:** Smith-Waterman algorithms are critical for gene sequencing, but they are inefficient when processing large amount of data. Existing heterogeneous acceleration methods suffer from high memory bandwidth and large hardware resource consumption.
- **Overview:** Designed PipeBSW, a hardware system which accelerates the Smith-Waterman algorithm on FPGA.
- **Contribution:** Optimized calculation cells to improve parallelism; Designed a hardware backtracking module to alleviate memory bottlenecks; Created a two-stage pipeline to reduce hardware resource consumption.
- **Result:** Achieved 720.9Mbps end-to-end throughput, and 58.4% LUT consumption reduction comparing to the baseline implementation with no pipeline structure.

RVDFI: A RISC-V Architecture with Security Enforcement by High Performance Complete Data-Flow Integrity (TC)

3rd author, Accepted — Nov 2020 – May 2021

Advisors: Prof. Zhongfeng Wang and Dr. Lang Feng

- **Motivation:** Data-flow integrity (DFI) is a security policy that enforces the legitimacy of all memory accesses. However, DFI verification requires intensive computation. Existing approaches implement partial DFI in order to lower the computational overhead.

- **Overview:** Established RVDFI, a secure RISC-V architecture which enables complete hardware-based DFI verification through specialized architecture design.
- **Contribution:** Optimized custom instruction formats to support the interaction between CPU cores and the DFI module; Improved the FIFO circuit design to speed up DFI verification.
- **Result:** Constructed the first complete DFI implementation based on RISC-V with 17.8% performance overhead, 50% less than previous designs.

PUBLICATIONS

PUBLISHED

[1] **Luyi Li**, Jun Lin, and Zhongfeng Wang, "PipeBSW: A Two-Stage Pipeline Structure for Banded Smith-Waterman Algorithm on FPGA," in *IEEE Computer Society Annual Symposium on VLSI* (**ISVLSI**), 2021 [**Best Paper Nomination**] [**Domain-specific Acceleration**] [**Conference**] [**Link**]

ACCEPTED

[1] **Luyi Li**, Jiayi Huang, Lang Feng, and Zhongfeng Wang "PREFENDER: A Prefetching Defender against Cache Side Channel Attacks as A Pretender," in *Design, Automation and Test in Europe* (**DATE**), 2022 [**Accepted**] [**Secure Computer Architecture**] [**Conference**] [**Link**]

[2] Lang Feng*, Jiayi Huang*, **Luyi Li**, Haochen Zhang, and Zhongfeng Wang "RVDFI: A RISC-V Architecture with Security Enforcement by High Performance Complete Data-Flow Integrity," in *IEEE Transactions on Computers* (**TC**), 2021 [*__Co-first Author__] [**Accepted**] [**Secure Computer Architecture**] [**Journal**] [**Link**]

SELECTED CLASS PROJECTS

A C- - Language Compiler Sep 2021 – Present

Principles and Techniques of Compilers Project

- Designed a compiler for C- - language, a simplified version of C language.
- Implemented main procedures in a compiler including lexical analysis, syntactic analysis, semantic analysis, IR generation, and object code generation.

A MIPS32 Processor Sep 2021 – Present

Computer Organization and Design Project

- Designed a processor based on MIPS32 Architecture in Chisel HDL.
- Implemented different design versions, include single-cycle processor, multi-cycle processor, and five-stage pipeline processor.

NEMU - A Full-system Intel i386 Emulator Mar 2021 – Jul 2021

Introduction to Computer System Project

- Repository: https://github.com/Owenlly/NJU_ICS_PA2021_Spring
- Designed and implemented NEMU, a complete full-system Intel i386 emulator in C.
- Implemented key features including a CPU core supporting x86 instruction set, a memory module with cache, segmentation and paging; Emulated interrupt, exception, and multiple I/O peripherals including a keyboard and a VGA monitor.

SKILLS

English Proficiency: TOEFL 105 (R28 L28 S22 W27), GRE 323 (V155 Q168) + AW3.5

Programming Language: C/C++, Python, Verilog/System Verilog, Chisel, Shell Script, LaTeX

Professional Software: MATLAB, Vivado Xilinx, Overleaf, Visio

Computer Architecture Tool: Gem5, RISC-V Toolchain